REMARKS

Claims 1, 3-15, 17-23, and 25 are pending in the present application. Reconsideration and allowance of pending claims 1, 3-15, 17-23, and 25 in view of the following remarks are requested.

A. Rejection of Claims 1, 3-15, 17-23, and 25 under 35 USC §103(a)

The Examiner has rejected claims 1, 3-15, 17-23, and 25 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,436,177 to Chiara Zaccherini (hereinafter "Zaccherini") in view of U.S. patent number 5,489,547 to Erdeljac et al. (hereinafter "Erdeljac") and U.S. patent number 6,156,602 to Shao et al. (hereinafter "Shao"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1 and 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao, singly or in any combination thereof.

The present invention, as defined by independent claim 1, includes, among other things, doping a layer over a transistor gate region with a first dopant, doping the layer over the transistor gate region and a field oxide region with a second dopant, and doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the transistor gate region is situated over a well and the field oxide region is not situated over the well. As disclosed in the present application, a first dopant (e.g. an N

type dopant) is implanted in a gate region of a polycrystalline layer, while a doping barrier prevents the first dopant from being implanted in a resistor region of the polycrystalline layer. As disclosed in the present application, after the doping barrier is removed, a second dopant (e.g. a P type dopant) is implanted in the polycrystalline layer to determine the resistivity of a resistor subsequently formed in the resistor region of the polycrystalline layer and also implanted in the gate region of the polycrystalline layer.

As disclosed in the present application, after a high resistivity resistor has been formed in the resistor region of the polycrystalline layer, a silicide blocking layer is formed over the resistor region, leaving portions of the resistor region uncovered by the silicide blocking layer. As disclosed in the present application, P+ doped regions are then formed by heavily doping the uncovered portions of the resistor region of the polycrystalline layer with a third dopant (e.g. a P type dopant) having the same conductivity type as the second dopant, and silicide contact regions are formed over the P+ regions to provide electrical connectivity for the high resistivity resistor. As a result of the above fabrication process, the present invention advantageously achieves a high resistivity resistor having a low fabrication cost and improved electrical connectivity.

In contrast to the present invention as defined by independent claim 1, Zaccherini does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dopant, doping the layer over the transistor gate region and a field oxide region with a second dopant, and doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, where

the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the transistor gate region is situated over a well and the field oxide region is not situated over the well. Zaccherini specifically discloses forming polycrystalline layer 7 over field oxide 5 and channel region 4, where field oxide 5 and channel region 4 are situated on epitaxial layer 3, which is situated on substrate 2. See, for example, column 2, lines 54-55, column 3, lines 1-14, and Figure 3 of Zaccherini. In Zaccherini, a P doped resistor is formed in predetermined area 8 of polycrystalline layer 7 overlying field oxide 5, while a gate terminal is formed over channel region 4. See, for example, column 3, lines 4-6 and 15-23 and Figure 4 of Zaccherini. In Zaccherini, the P doped resistor and the gate terminal are both situated over epitaxial layer 3.

Thus, Zaccherini fails to teach, disclose, or suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region, as specified in independent claim 1. Furthermore, as disclosed in the present application, the well and the field oxide region are formed in a silicon substrate. In contrast, in Zaccherini a field oxide region is formed in epitaxial layer 3, which is formed on substrate 2. Thus, the structure disclosed in Zaccherini is substantially different than the structure disclosed in the present application. As disclosed in the present application, an embodiment of the present invention does not require the additional processing steps of forming and doping an epitaxial layer on a

substrate, as required in Zaccherini. Furthermore, Zaccherini provides no motivation for forming a field oxide region and a well directly in a substrate.

Additionally, Zaccherini fails to teach, disclose, or suggest doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, as specified in independent claim 1. Moreover, Zaccherini provides no motivation for forming a high-doped region in the layer over the field oxide region. In fact, Zaccherini does not even mention any method of completing formation of the P doped resistor formed in predetermined area 8 of polycrystalline layer 7.

In contrast to the present invention as defined by independent claim 1, Erdeljac does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dopant, doping the layer over the transistor gate region and a field oxide region with a second dopant, and doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the transistor gate region is situated over a well and the field oxide region is not situated over the well. Erdeljac specifically discloses resistors 32 and 34 formed on field oxide region 20, which is formed over P- epitaxial layer 12, and gate 24, which is formed over N well 18 in P- epitaxial layer 12. See, for example, column 1, lines 46-67, column 2, lines 1-6, and Figure 11 of Erdeljac. In Erdeljac, a first polysilicon layer is deposited over field oxide region 20 and gate oxide

layer 22, heavily doped with an N type dopant, and patterned and etched to form gate 24. See, for example, Erdeljac, column 1, lines 62-65 and column 2, lines 1-10.

In Erdeljac, second polysilicon layer 28 is deposited over gate 24 and field oxide region 20, lightly doped with an N type dopant, and patterned and etched to form resistors 32 and 34 on field oxide region 20. See, for example, column 2, lines 15-23, column 5, lines 24-26, and Figures 3 and 11 of Erdeljac. Thus, in Erdeljac, resistors 32 and 34 have the same conductivity type (i.e. N type). Furthermore, in Erdeljac, resistors 32 and 34 are formed in second polysilicon layer 28 while gate 24 is formed in a first polysilicon layer. However, Erdeljac fails to teach, disclose, or suggest doping a layer over a transistor gate region with a first dopant, doping the layer over the transistor gate region and a field oxide region with a second dopant, and doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the transistor gate region is situated over a well and the field oxide region is not situated over the well, as specified in independent claim 1. Thus, Erdeljac fails to cure the basic deficiencies of Zaccherini discussed above.

Also, the resulting structure in Erdeljac, which includes gate 24 and resistors 32 and 34, is substantially different than the structure disclosed in Zaccherini. For example, Zaccherini discloses forming a P doped resistor and a gate terminal in the same polycrystalline layer (i.e. polycrystalline layer 7). In contrast, in Erdeljac, gate 24 is

formed in a first polysilicon layer while resistors 32 and 34 are formed in a second polysilicon layer (i.e. second polysilicon layer 28). Thus, for the above reasons, Applicant respectfully submits that there is not sufficient motivation to combine Zaccherini and Erdeljac, as the Examiner suggests. In particular, there is insufficient motivation to modify Zaccherini by forming a well as disclosed in Erdeljac.

In contrast to the present invention as defined by independent claim 1, Shao does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dopant, doping the layer over the transistor gate region and a field oxide region with a second dopant, and doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the transistor gate region is situated over a well and the field oxide region is not situated over the well. Shao specifically discloses performing N+ implant 18 into poly 2 layer 16 to form the conductivity level of an NMOS poly gate and also to control the value of a load resistor (i.e. load resistor 38), which is also formed in poly 2 layer 16 over field oxide region 12. See, for example, column 5, lines 7-26 and Figures 1 and 5 of Shao. In Shao, NMOS gate 40 and load resistor 38 are both situated over substrate 10. See, for example, Figure 5 of Shao. However, Shao fails to teach, disclose, or suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region, as specified in independent claim 1.

Also, in Shao, an N+ implant is used to dope poly 2 layer 16, which is subsequently patterned and etched to form load resistor 38 and NMOS gate 40. Thus, in contrast to the present invention, load resistor 38 and NMOS gate 40 are not independently doped. Furthermore, Shao does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dopant having a first conductivity type and doping the layer over the transistor gate region and over a field oxide region with a second dopant having a second conductivity type, as specified in independent claim 1. In addition, Shao fails to teach, disclose, or suggest forming a doping barrier above the layer over the field oxide region (i.e. the resistor region) prior to doping the layer over the transistor gate region, as specified in independent claim 1. Moreover, Shao fails to teach, disclose, or suggest utilizing a first dopant to dope a transistor gate region, utilizing a second dopant to form a high resistivity resistor in a layer over a field oxide region, and utilizing a third dopant to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, as specified in independent claim 1.

On page 4 of the Office Action dated December 1, 2004, the Examiner has stated that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zaccherini and Erdeljac with the teachings of Shao. However, the structures and methods of forming the respective structures disclosed in Zaccherini, Erdeljac, and Shao are substantially different from each other. Thus, Applicant respectfully submits that there is not sufficient motivation for modifying

Zaccherini in view of Erdeljac, and Shao as suggested by the Examiner. In particular, the Examiner has not provided sufficient motivation to modify Zaccherini to include the well as disclosed in Erdeljac. Thus, Applicant respectfully submits that the combined teachings suggested by the Examiner are based on a classic hindsight reconstruction given the benefit of Applicant's disclosure, which is impermissible.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao, singly or in any combination thereof. As such, the present invention, as defined by independent claim 1, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus claims 3-13 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by independent claim 14, teaches, among other things, doping a polycrystalline silicon layer over a gate region with a first dopant, doping the polycrystalline silicon layer over the gate region and a resistor region with a second dopant, and doping a portion of the resistor region of the polycrystalline silicon layer with a third dopant so as to form a high-doped region in the resistor region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, and where the gate region is situated over a well and the resistor region is not situated over the well. Independent claim 14 includes similar limitations as recited

in independent claim 1. Thus, for similar reasons as discussed above, Applicant respectfully submits that the present invention, as defined by independent claim 14, is not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao. As such, the present invention, as defined by independent claim 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus claims 15, 17-23, and 25 depending from independent claim 14 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 14, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 3-15, 17-23, and 25 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 3-15, 17-23, and 25 pending in the present application is respectfully requested.

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Respectfully Submitted,
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